instruction, wherein said second instruction is selected from said group of potentially valid instructions, and wherein said second instruction further comprises an instruction that does not utilize the same system resources other than source registers utilized by said first instruction, or from an ordered instruction list in said user preference queue, wherein each instruction selected comprises either the next instruction in said ordered instruction list or a "no operation" instruction if said next instruction in said ordered instruction list requires unavailable system resources or violates the processor grouping rules; and

generating and simulating instructions that correspond to said group of N instructions created by said instruction packer, evaluating the updated architectural state of the golden model, and updating said resource-related data structures.

REMARKS

Drawings

Figures 1 and 2 stand objected to under MPEP § 608.02(g) for illustrating only the prior art without an appropriate legend indicating the same. Figures 1 and 2 have been amended to include the following legend: "Prior Art".

Withdrawal of the objection is respectfully requested.

Specification

The specification stands objected to because of informalities relating to references to additional patent applications which lacked applicable serial and related registration numbers. The specification has been amended to correct the cited informalities.

Withdrawal of the objection is respectfully requested.

Claims

Claims 1-30 were pending and examined. The Examiner rejected claims 1-30 under 35 U.S.C. §102(e) as being as anticipated by Chin et al. (USPN 6,484,135). In this response Applicant has amended claims 1, 6, 11, 16, 21, 26, 27, 28, 29, and 30. Claims 1-30 are pending.

Claim rejection under 35 U.S.C. Section 102(e)

The Examiner rejected claims 1-30 under 35 U.S.C. § 102(e) as being anticipated by Chin. In response to these rejections, Applicant has amended the independent claims (1, 6, 11, 16, 21, 26, 27, 28, 29, and 30) as indicated above to recite explicitly that the generated test is a program capable of being executed by the processor and that the information concerning selected system resources of the golden model represented within the plurality of resource-related data structures comprises two or more of the applicable states for the system resources. Support for this amendment is found in the specification in the paragraph beginning on page 20, line 18; the paragraph beginning on page 21, line 2; the paragraph beginning on page 23, line 18; and the description of resource tracking beginning on page 26, line 14.

Applicant respectfully submits that the cited reference neither anticipates nor suggests a method and apparatus for verifying that a processor under test properly executes two or more instructions issued and executed in parallel as recited in independent claims 1, 6, 11, 16, 21, 26, 27, 28, 29, and 30 as amended herein. Chin discloses an apparatus for adoptively generating test vectors (i.e., patterns of data representing various system states) (Chin column 1, line 40 and column 2, lines 2-5) to verify the behavior of a generalized digital system. Chin, however, neither teaches nor suggests the generation of machine executable programs for the examination and verification of processors, and in particular, the unique case of processors that execute programs containing two or more instructions in parallel.

Whereas the apparatus and method of Chin analyzes only the current internal state information of the generalized digital system under test to generate adaptive test vectors, claims 1, 6, 11, 16, 21, 26, 27, 28, 29, and 30 (as amended herein) recite an apparatus and method for generating a test program for processor verification having a user preference queue and an instruction packer coupled to the user preference queue for analyzing at least two states of the system under test (i.e.,

more than just the current internal state information of the applicable system) and generating a group of instructions valid for parallel execution by the processor.

While Chin discloses the use of system states, the disclosure references "current internal model state information." Chin at column 5, lines 4-6 and 9-12. Further, while Chin does disclose a test generator for generating test or input vectors, no where does Chin disclose or otherwise suggest generation of test programs wherein the instructions included within the program have been verified for parallel execution. In contrast, Applicant's apparatus and method generates test programs for processor verification by dynamically tracking selected system resources (including historical, current, and predicted resource availability and system states) wherein the test programs include groups of instructions designated for parallel execution on the processor system under test. The ability to test and verify a processor's ability to execute valid instructions in parallel is a highly desirable feature, and not one that is disclosed in or otherwise taught by Chin.

In Chin, the generated test vectors may be concurrently applied to both a hardware model and a hardware emulator of a digital system. Chin at column 5, lines 14-16. In this manner, the applicable test vectors may be sequentially applied to two different representations of the same system (i.e., a hardware model which is a relatively detailed, low-level software characterization of the corresponding general digital system and a hardware emulator which is a relatively high-level software characterization of the corresponding general digital system), not executed in parallel by the same system. Chin at column 5, lines 16-24. Consequently, Chin neither teaches nor suggests using the test generator to select test programs by first defining potential groups of instructions appropriate for parallel execution and then selecting instructions from those groups for parallel execution by the processor under test for comparison and verification. In sharp contrast, independent claims 1, 6, 11, 16, 21, 26, 27, 28, 29, and 30 as amended herein recite explicitly that the generated test programs are valid for parallel execution by the processor system under test.

Because the cited reference fails to disclose a method and apparatus for generating test programs to verify that a processor under test properly executes two or more instructions issued and executed in parallel, the limitations of amended independent claims 1, 6, 11, 16, 21, 26, 27, 28, 29, and 30 are neither anticipated nor suggested by the cited reference. Therefore, Applicant respectfully requests the Examiner to reconsider and withdraw the prior art rejection of independent

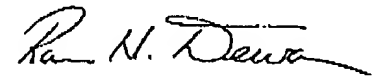
claims 1, 6, 11, 16, 21, 26, 27, 28, 29, and 30. Further and in accordance with *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988) and TMEP § 2143.03, if the prior art rejection of independent claims 1, 6, 11, 16, 21, 26, 27, 28, 29, and 30 is withdrawn, then all claims depending therefrom are non-obvious as well. Accordingly, Applicant also respectfully requests the Examiner to withdraw the prior art rejection of dependent claims 2-5, 7-10, 12-15, 17-20, and 22-25.

In summary, the basic device taught by Chin neither discloses nor suggests a method and apparatus for generating a test program for processor verification comprising a user preference queue and an instruction packer coupled to the user preference queue for analyzing at least two states of the system under test and generating a group of instructions valid for parallel execution by the processor under test. Chin does not motivate one to generate instructions valid for parallel execution. On the contrary, Chin is directed towards generating test vectors for sequential use in the validation of generalized digital systems. The limitations of the claimed invention relating to generating test programs that enable the verification of whether a processor system under test properly executes two or more instructions issued and executed in parallel clearly distinguish the claimed invention from the invention depicted in Chin.

CONCLUSION

In the present response, Applicant has responded to the Examiner's objection to Figures 1 and 2, the cited informalities contained in the specification, and rejection of pending claims 1-30 under 35 U.S.C. §§ 102(e). Accordingly, Applicant believes that this response constitutes a complete response to each of the issues raised in the Office Action. In light of the amendments made herein and the accompanying remarks, Applicant believes that pending claims 1-30 are in condition for allowance. Accordingly, Applicant respectfully requests the Examiner to withdraw the rejections, allow the pending claims, and advance the application to issue. If the Examiner has any questions, comments, or suggestions, the undersigned attorney would welcome and encourage a telephone conference at 512.236.2335.

Respectfully submitted on behalf of Applicant,



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